RESTATEMENT OF PENDING CLAIMS

1. (Original) An image processing apparatus comprising:

a memory circuit storing an input data in response to a write address and outputting an output data in response to a read address;

a one-line judging circuit receiving a horizontal synchronization signal and a sampling clock signal, the one-line judging circuit comparing a number of pixels sampled within one line of the horizontal synchronization signal with a predetermined number so as to output a comparison signal and a difference signal representing a difference between the sampled number of pixels and a predetermined number;

a write control circuit coupled to the memory circuit and the one-line judging circuit, the write control circuit generating the write address in response to the sampling clock signal and the comparison signal and a read control signal in response to the comparison signal; and

a read control circuit coupled to the memory circuit, the write control circuit and the one-line judging circuit, the read control circuit generating the read address in response to the write address, the read control signal and the difference signal.

2. (Original) An image processing apparatus according to claim 1, wherein a storage capacity of the memory circuit is smaller than the number of pixels sampled within one line of the horizontal synchronization signal.

3. (Original) An image processing apparatus according to claim 1, wherein the one-line judging circuit includes

a counter counting the sampling clock signal in response to the horizontal synchronization signal, and

a pixel determination circuit coupled to the counter for generating the comparison signal and the difference signal in response to an output signal from the counter.

4. (Original) An image processing apparatus according to claim 1, wherein the write control circuit includes

a control circuit generating a write counter control signal and the read control signal in response to the comparison signal, and

a write counter generating the write address in response to the sampling clock signal and the write counter control signal.

5. (Original) An image processing apparatus according to claim 1, wherein the write control circuit receives the difference signal.

6. (Original) An image processing apparatus according to claim 1, wherein the read control circuit includes

a control circuit receives the write address and the read control signal and generates a read address in response to the received signals,

a register stores the write address and the difference signal and outputs the stored write address,

a read adjusting circuit compares the write address received from the control circuit with the stored write signal received from the register and outputs a switching signal in response to the comparison thereof, and

a selection circuit selectively outputs the write address received from the control circuit or the stored write signal received from the register in response to the switching signal.

7. (Original) An image processing apparatus according to claim 6, wherein the control circuit includes

a reading control circuit receives the write address and the read control signal and generates a read counter control signal in response to the received signals, and

a read counter outputs the read address in response to the read counter control signal and the sampling clock signal.

8. (Original) An image processing apparatus comprising:

a memory circuit having a capacity of n, the memory circuit storing an input data in response to a write address and outputting an output data in response to a read address;

a counter counting a sampling clock signal in response to a horizontal synchronization signal and outputting a counting signal;

a write control circuit coupled to the memory circuit and the counter, the write control circuit generating the write address in response to the sampling clock signal, the horizontal synchronization signal and the counting signal; and

a read control circuit coupled to the memory circuit and the write control circuit, the read control circuit generating the read address in response to the write address, the sampling clock signal and a phase difference signal representing n/2, wherein n is a natural number.

9. (Original) An image processing apparatus according to claim 8, wherein the write control circuit includes

a control circuit generating a write counter control signal in response to the counting signal, and

a write counter generating the write address in response to the sampling clock signal, the horizontal synchronization signal and the write counter control signal.

10. (Original) An image processing apparatus according to claim 8, wherein the write control circuit compares the counting signal with the horizontal synchronization signal.

11. (Original) An image processing apparatus according to claim 8, wherein the read control circuit includes

a control circuit receives the write address and the phase difference signal and generates the read address in response to the received signals, the control circuit stopping generation of the read address in response to an output prohibit signal, and

an address determination circuit compares the read address received from the control circuit with the write signal received from the write control circuit and outputs the output prohibit signal when the read address received from the control circuit is coincident with the write signal received from the write control circuit.

12. (Original) An image processing apparatus according to claim 11, wherein the control circuit includes

a reading control circuit receives the write address and the phase difference signal and generates a read counter control signal in response to the received signals, and

a read counter outputs the read address in response to the read counter control signal and the sampling clock signal, the read counter stopping generation of the read address in response to the output prohibit signal.

13. (Original) An image processing apparatus according to claim 11, wherein the control circuit is reset in response to a horizontal synchronization signal received thereto.

14. (Original) An image processing apparatus according to claim 12, further comprising a logic circuit providing the read control signal and the output prohibit signal in response to a horizontal synchronization signal received thereto.

15. (Original) An image processing apparatus comprising:

a memory circuit having a capacity of n, the memory circuit storing an input data in response to a write address and outputting an output data in response to a read address;

a counter counting a sampling clock signal in response to a horizontal synchronization signal and outputting a counting signal;

a write control circuit coupled to the memory circuit and the counter, the write control circuit generating the write address in response to the sampling clock signal, the horizontal synchronization signal and the counting signal; and

a read control circuit coupled to the memory circuit and the write control circuit, the read control circuit generating the read address when the read control circuit detects a phase difference representing n/2 based on the write address and the sampling clock signal, wherein n is a natural number.

16. (Original) An image processing apparatus according to claim 15, wherein the write control circuit includes

a control circuit generating a write counter control signal in response to the counting signal, and

a write counter generating the write address in response to the sampling clock signal, the horizontal synchronization signal and the write counter control signal.

17. (Original) An image processing apparatus according to claim 15, wherein the write control circuit compares the counting signal with the horizontal synchronization signal.

18. (Original) An image processing apparatus according to claim 15, wherein the read control circuit includes

a control circuit generates the read address in response to the write address and the sampling clock signal, the control circuit stopping generation of the read address in response to an output prohibit signal, and

an address determination circuit compares the read address received from the control circuit with the write signal received from the write control circuit and outputs the output prohibit signal when the read address received from the control circuit is coincident with the write signal received from the write control circuit.

19. (Original) An image processing apparatus according to claim 18, wherein the control circuit includes

a reading control circuit receives the write address and generates a read counter control signal in response to the write address, and

a read counter outputs the read address in response to the read counter control signal and the sampling clock signal, the read counter stopping generation of the read address in response to the output prohibit signal.

20. (Original) An image processing apparatus according to claim 18, wherein the control circuit is reset in response to a reset signal received from an outside.